Characterization of Transistor Matching in Silicon-Germanium Heterojunction Bipolar Transistors

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Characterization of Transistor Matching in Silicon-Germanium Heterojunction Bipolar Transistors

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SUMMARY

Device mismatch is crucial in many types of analog circuits, including differential pairs for the input stages of amplifiers, current mirrors for biasing, and in various circuits topologies utilizing integer multiples of identical components such as bandgap references, ADCs, DACs, and filters. Thus, accurate transistor matching is at the very heart of robust analog circuit design. Chapter II explores the fundamentals of device mismatch and explores for the first time the geometric dependence of collector current variations in SiGe HBTs. Chapter III examined the effects of radiation on various SiGe HBT BiCMOS technologies. The space community is increasingly using COTS parts in spaceborne systems, thus radiation testing on new commercial technologies is imperative. The effects of proton irradiation on matched device pairs on a new commercially-available SiGe technology were examined for the first time. Chapter IV presents the results of the effects of collector current mismatch at high temperatures. As such, device mismatch effects at high-temperature have not been seriously studied. This is probably because the temperature effects are believed to be insignificant to transistor mismatch. This characteristic is essential in order to prove its applicability in high-temperature precision analog circuits.

CHAPTER I

INTRODUCTION

1.1 Motivation

In today's fast growing markets, analog and digital signal processing (DSP) are the key technologies fueling innovative, high-growth applications. Such applications include digital wireless, broadband access, digital audio, high-resolution imaging and motor control. As the interface between digital and "real-world" signals, analog chips play an integral role in most electronic equipment. For example, depending on the system, for every DSP in an electronic system, there are approximately ten analog components. As a result, analog technology is an engine driving the Information age with high-growth applications such as wireless and broadband communications, consumer audio and video, and PC peripherals.

Due to the broad spectrum of analog applications, the analog IC market is a highly fragmented and competitive sector of the semiconductor industry. The Semiconductor Industry Association (SIA) estimated the analog market at $31.3 billion in 2004 and forecasts it to grow to $33.7 billion in 2006. This growth pattern fuelled by the increasing need for high-performance analog in digital systems has led to increase in complexity and capability of analog ICs. In order, to accommodate the accelerating need for faster and cheaper DSP, high performance and cost effective analog ICs will be required. This task places new requirements on technology, and poses new challenges for technologists.

Due to the rapid expansion of the analog IC market, technologists venture towards higher performance devices while maintaining lower costs. Traditionally, analog circuits required much higher power supply levels [3]. This deemed Sige HBTs unsuitable since high BV_{CEO} came at a cost of poor high frequency performance. However, due to declining analog voltage levels, SiGe has developed a niche in the analog IC market. This technology

provides low power, low noise, and high frequency analog solutions in comparison to Si-only technology [2]. With aggressive design efforts and shrinking device sizes, parasitics such as device mismatch limit circuit performance.

In general, transistor "mismatch" refers to the measurable differences in electrical characteristics (e.g., I_C, β, or g_m) between two identically designed and layed-out devices, which are biased identically, and placed in very close proximity on the wafer to minimize cross-wafer process variations (this is often called a "matched pair"). Matched pairs are critical in many types of analog circuits, including differential pairs for the input stages of amplifiers, current mirrors for biasing, and in various circuits topologies utilizing integer multiples of identical components such as bandgap references, ADCs, DACs, and filters. Thus, accurate transistor matching is at the very heart of robust analog circuit design.

The primary goal of this thesis will be to investigate the transistor level static performance implications of device mismatch of SiGe HBT BiCMOS technology. We will try to achieve this goal by presenting and analyzing the *dc* characterization results of various device geometries under extreme conditions such as radiation and a range of temperatures.

1.2 SiGe HBT BiCMOS Technology

Silicon-Germanium (SiGe) heterojunction bipolar transistor (HBT) technology uses Si-based bandgap engineering to provide high speed, low noise, and power efficient devices in a high-yielding, low cost IC platform. SiGe BiCMOS technology offers high-performance SiGe HBTs and passive component capabilities combined with deep sub-micron CMOS. The SiGe HBT uses bandgap engineering to achieve III-V like performance while maintaining compatibility with conventional Si CMOS manufacturing. This technology allows for system-on-a-chip (SoC) integration. As a result, SiGe technology is rapidly becoming a popular choice for analog, digital, radio frequency (RF), microwave, and millimeter wave integrated circuit applications.

Silicon-Germanium (SiGe) is a new technology that combines the integration and cost

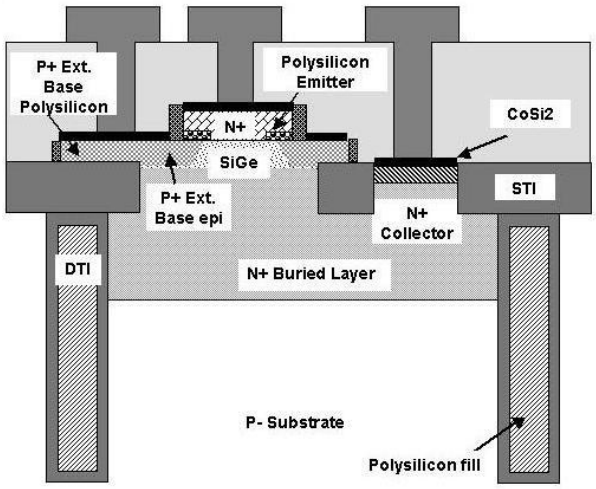

Figure 1: A schematic cross-section of the SiGe HBT.

benefits of silicon with the speed of more esoteric and expensive technologies such as gallium-arsenide. The key difference between SiGe HBTs and Si BJTs is the introduction of SiGe epi layer into the base of an otherwise all-silicon bipolar transistor. The base region is thus comprised of a Si buffer, boron-doped graded SiGe alloy active layer, and a Si cap. Figure 2 depicts a SIMS doping and Ge profile for a representative first generation SiGe HBT.

The inclusion of graded SiGe alloy in the base facilitates bandgap engineering for use in tailoring npn bipolar transistors. The compressive strain associated with SiGe alloy produces an additional bandgap shrinkage which improves carrier mobility in comparison to Si BJTs. This leads to lower base resistance and improved dynamic response [1]. The trade-off in SiGe epitaxial growth involves balancing of two competing temperature dependent requirements, namely, mobility of the adhering atomic species and formation of dislocation nucleation. As for increased mobility, large temperatures are preferred, but to avoid strain relaxation by enhanced dislocation formation, low temperatures are necessary. Several techniques have been developed for the growth of SiGe epitaxial films. The list includes MBE, [34] and [35], limited Reaction Processing (LRP) or Rapid thermal Chemical Vapor Deposition (RTCVD) [36], Atmospherice Pressure Chemical Vapor Deposition

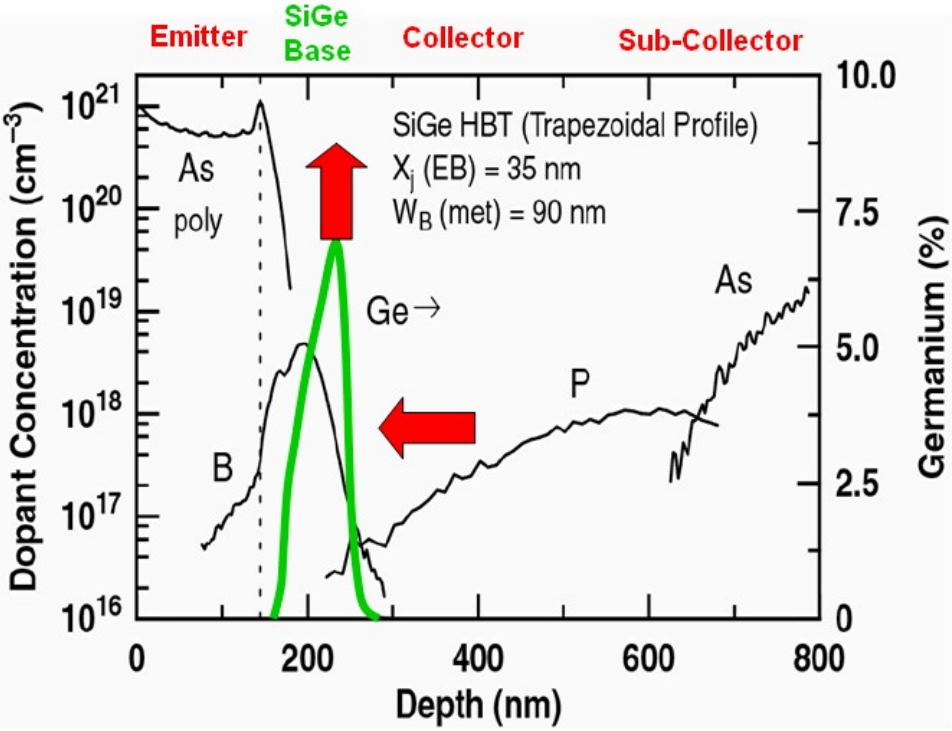

Figure 2: Representative SIMS profile for a first generation SiGe HBT.

(APCVD) [37], and ultra-high vacuum/chemical vapor deposition (UHV/CVD) [38]. The UHV/CVD is a more widely used technique for SiGe epitaxial growth since it eliminates the high thermal budget of conventional epitaxy by chemical means.

The SiGe BiCMOS technology under investigation is the commercially-available National BiCMOS8 SiGe HBT process technology. The SiGe HBT utilizes deep trench isolation, a self-aligned emitter-base structure, in-situ doped polysilicon emitter, and a non-selective SiGe epitaxial base process. The process features six layers of metalization and includes 2.5V CMOS devices. The SiGe HBTs have a 0.4μm emitter stripe width, a nominal peak f_T of 60GHz, a peak f_{max} of 60-70GHz, and a BV_{CEO} of 3.3V. A schematic cross-section of the SiGe HBT is shown in Figure 1 and a SEM cross-section is depicted in Figure 4.

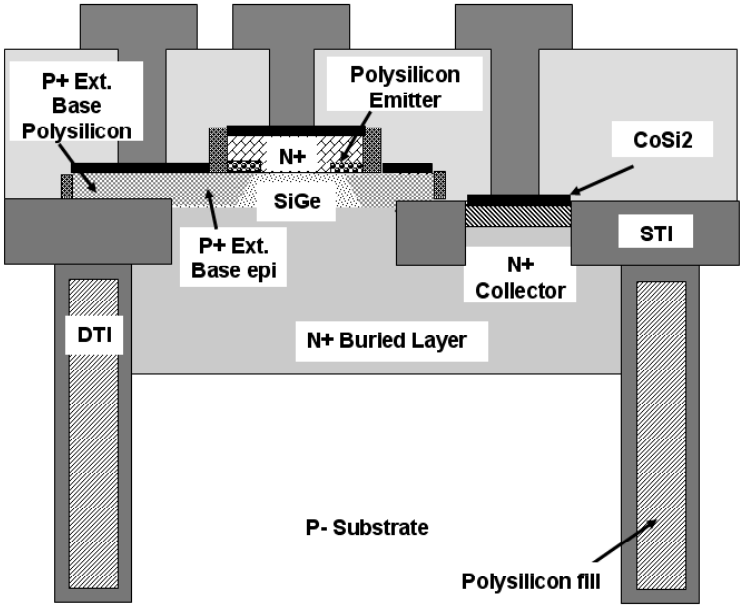

Figure 3: A schematic device cross-section of the National BiCMOS8 SiGe HBT under investigation.

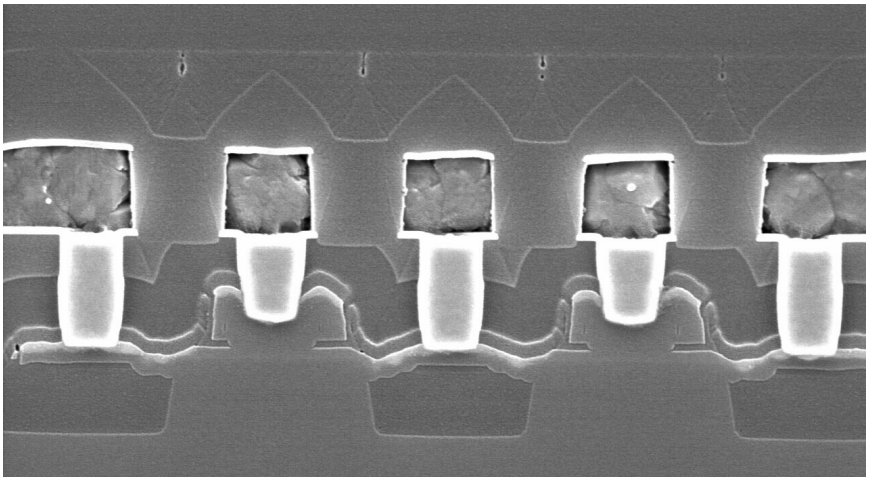

Figure 4: SEM device cross-section of the National BiCMOS8 SiGe HBT under investigation.

Table 1: Target device parameters for National SiGe BiCMOS technology.

SiGe BiCMOS Technology	National BiCMOS8
SiGe HBT Parameters	
Drawn Emitter Width (μm)	0.4
V_A (V)	175
BV_{CEO} (V)	3.3
Peak f_T (GHz)	60
Peak f_{max} (GHz)	60-70
nFET Parameters	
Channel L (μm)	0.24
V_{DD} (V)	2.75

1.3 SiGe Device Physics

As earlier mentioned, SiGe alloy is introduced into the base of a Si BJT by means of pseudomorphic growth of strained SiGe on Si. This process sucessfully utilises bandgap engineering in the Si material system to achieve III-V like performance while maintaining compatibility with conventional Si CMOS manufacturing.

From a performance perspective, introducing Ge into Si improves speed, current gain, linearity and noise characteristics. However, from a physical perspective, the difference in lattice constants between Ge and Si result in SiGe having a slightly higher lattice constant that Si. Ge has a smaller bandgap energy than Si (0.66 eV and 1.12 eV respectively), consequently SiGe has a smaller bandgap than Si facilitating bandgap engineering in Si. The compressive strain in the SiGe film produces an additional bandgap shrinkage resulting in about 75meV reduction in bandgap for every 10% of Ge introduced. Since this b̈and offsetöccurs primarily in the valence band, Si npn BJTs can be tailored to obtained required performance metrics. The compressive strain also lifts the conduction and valence band degeneracies at the band extremes. This effectively reduces the density-of-states and improves carrier mobilities.

The presence of Si-SiGe heterojunctions in the emitter-base (EB) and collector-base (CB) junctions of the SiGe HBT results in a marked performance improvement in both

dc and *ac* characteristics over the Si BJT. The energy band diagram for a forward biased graded-base SiGe HBT and a comparable Si BJT is shown in Figure 5. The effect of graded Ge content in the base is apparent in the band structure changes shown above. A slight reduction in the base bandgap at the EB junction ($\Delta E_{g,Ge}(x = 0)$) and a much larger reduction at the CB junction ($\Delta E_{g,Ge}(x = W_b)$) is observed. This grading of Ge across the base induces a built-in quasi-drift field ((($\Delta E_{g,Ge}(x = W_b)$)-($\Delta E_{g,Ge}(x = 0)$))/W_b) in the neutral base region, positively impacting the minority carrier transport.

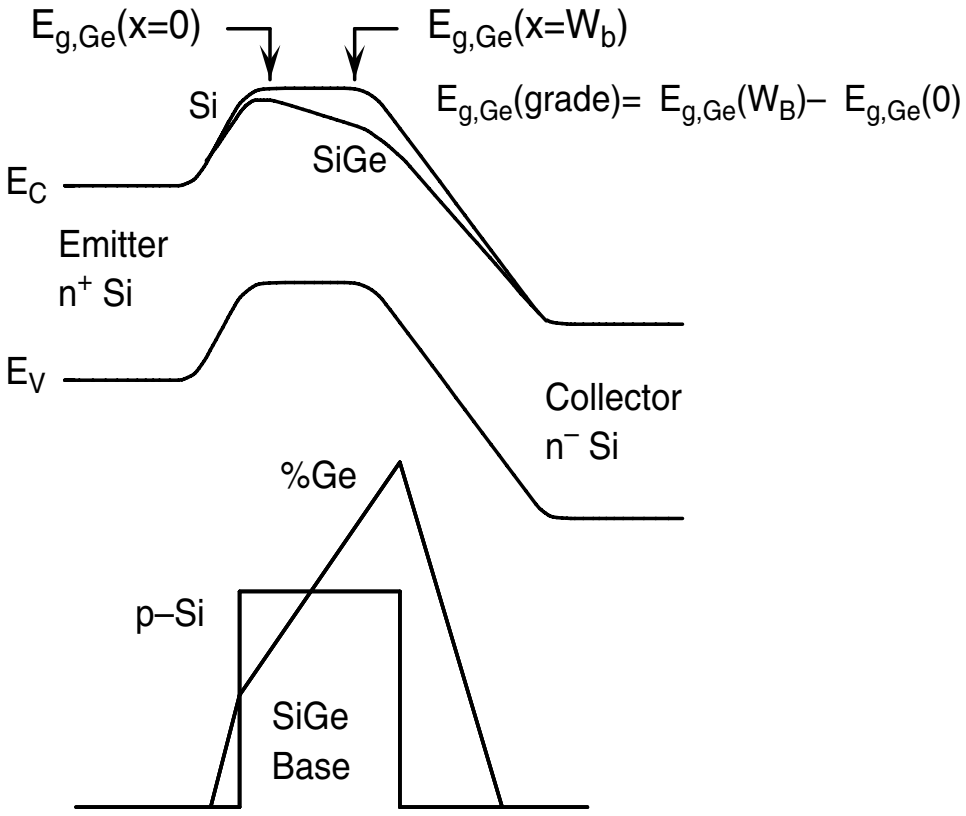

Figure 5: Energy band diagram for a graded base SiGe HBT and a Si BJT.

From Figure 5, we see that the emitter-base potential barrier is reduced in the SiGe HBT with respect to the Si BJT, thereby allowing increased electron injection from emitter to base. The enhanced electron injection leads to a higher collector current and current gain. An expressions for the collector current density (J_C) can be derived in closed-form

from the generalized Moll-Ross J_C relation [8],

$$J_C = \frac{q(e^{qV_{BE}/kT-1})}{\int_0^{W_b} \frac{p_b(x)dx}{D_{nb}(x)n_{ib}^2(x)}} \tag{1}$$

where W_b is the neutral base width for the applied bias V_{BE}, $p_b(x)$ is the base doping, and D_{nb} is the minority electron diffusivity in the base. The intrinsic carrier density in the SiGe HBT is given by

$$n_{ib}^2 = \gamma n_{io}^2 e^{\Delta E_{gb}^{app}/kT} e^{[\Delta E_{g,Ge}(grade)]x/(W_b kT)} e^{\Delta E_{g,Ge}(0)/kT} \tag{2}$$

where $\Delta E_{gb}^{app}/kT$ is the apparent bandgap narrowing due to heavy doping in the base and define $\Delta E_{g,Ge}(grade)$ as $\Delta E_{g,Ge}(W_b) - \Delta E_{g,Ge}(0)$. The low-doping intrinsic carrier density for Si is $n_{io}^2 = N_C N_V e^{-E_{go}/kT}$ and $\gamma = (N_C N_V)_{SiGe}/(N_C N_V)_{Si} < 1$ is the effective density-of-states ratio between SiGe and Si [23]. An expression for J_C in a SiGe HBT can be obtained using Equation 2 into 1[24], [25]:

$$J_{C,SiGe} = \frac{qD_{nb}}{N_{ab}^- W_b} \left(e^{qV_{BE}/kT} - 1\right) n_{io}^2 e^{\Delta E_{gb}^{app}/kT} \left\{ \frac{\widetilde{\gamma}\widetilde{\eta} e^{\Delta E_{g,Ge}(0)/kT} \Delta E_{g,Ge}(grade)/kT}{1 - e^{-\Delta E_{g,Ge}(grade)/kT}} \right\} \tag{3}$$

where "$\sim$" is a position-averaged quantity, N_{ab}^- is the ionized doping level in the base, and $\tilde{\eta} = \left(\widetilde{D_{nb}}\right)_{SiGe} / (D_{nb})_{Si} > 1$ is the minority electron diffusivity ratio between SiGe and Si. Note the first term in Equation 3 corresponds to the Si BJT and the second term represents the modification of J_C due to the Ge content in the base. Figure 6 depicts the Gummel characteristics for a typical SiGe HBT and a similarly constructed Si BJT. As expected, the SiGe HBT exhibits higher collector current and approximately the same base current as the Si BJT. The increase in J_C for the SiGe HBT in turn leads to an increase in current gain (β). The current gain ratio between a SiGe HBT and an identically constructed Si BJT can be expressed as:

$$\frac{\beta_{SiGe}}{\beta_{Si}} \cong \frac{J_{C,SiGe}}{J_{C,Si}} = \frac{\widetilde{\gamma}\widetilde{\eta} \Delta E_{g,Ge}(grade)/kT e^{\Delta E_{g,Ge}(0)/kT}}{1 - e^{-\Delta E_{g,Ge}(grade)/kT}} \tag{4}$$

The current gain depends linearly on the band offset due to Ge grading across the base and exponentially on the Ge induced band offset at the EB junction as Equation 4 indicates.

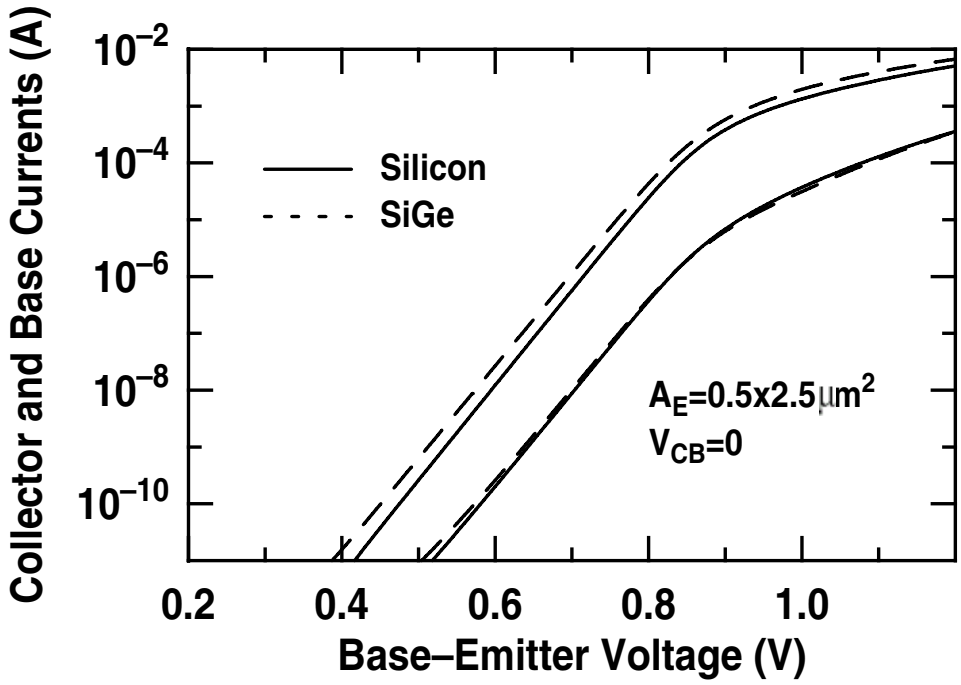

Figure 6: Representative Gummel plot for a SiGe HBT as compared to a Si BJT.

Therefore, β is dependent on the Ge profile shape and can be modified for particular circuit applications. The introduction of Ge in the base in effect decouples β from the base doping. This fact implies that the base doping can be increased with out degrading β. Note that higher base doping reduces the base resistance which has positive implications in terms of frequency response and broadband noise.

The output conductance is an important design parameter for analog circuits and is conveniently described by the Early voltage (V_A). A graded Ge profile in the base of the SiGe HBT leads to the enhancement of V_A that of the Si BJT as shown below:

$$\frac{V_{A,SiGe}}{V_{A,Si}} \Big|_{V_{BE}} = e^{\Delta E_{g,Ge}(grade)/kT} \left[\frac{1 - e^{-\Delta E_{g,Ge}(grade)/kT}}{\Delta E_{g,Ge}(grade)/kT} \right] \tag{5}$$

The Early voltage depends exponentially on the Ge grading across the base, which decouples V_A from the base doping and hence β. Consequently a high "current-gain–Early voltage product" (βV_A product), a figure-of-merit for analog applications, can be maintained independent

of the base profile.

$$\frac{\beta V_{A,SiGe}}{\beta V_{A,Si}} = \widetilde{\gamma}\widetilde{\eta} e^{\Delta E_{g,Ge}(0)/kT} e^{\Delta E_{g,Ge}(grade)/kT} \tag{6}$$

Note that the βV_A product for the SiGe HBT is enhanced over the Si BJT and is an exponential function of the band offset at the EB junction as well the Ge grading across the base.

Two important *ac* figures-of-merit are the unity-gain cutoff frequency (f_T) and the maximum oscillation frequency (f_{max}). Both parameters are positively impacted by the Ge content in the base as will be shown below. The unity-gain cutoff frequency is given by:

$$f_T = \frac{1}{2\pi}\left[\frac{1}{g_m}(C_{eb} + C_{cb}) + \tau_b + \tau_e + \frac{W_{CB}}{2v_{sat}} + r_c Ccb\right]^{-1} \tag{7}$$

where g_m is the intrinsic transconductance, C_{eb} and C_{cb} are the EB and CB depletion capacitances, τ_b is the base transit time, τ_e is the emitter charge storage delay time, W_{CB} is the CB space-charge region width, v_{sat} is the saturation velocity, and r_c is the collector resistance. The grading of Ge across the base induces a built-in electric field in the neutral base region (directed from collector to emitter). This field accelerates the minority carriers across the base which effectively reduces the base transit time.

$$\frac{\tau_{b,SiGe}}{\tau_{b,Si}} = \frac{2}{\widetilde{\eta}} \frac{kT}{\Delta E_{g,Ge}(grade)} \left\{1 - \frac{kT}{\Delta E_{g,Ge}(grade)}\left[1 - e^{-\Delta E_{g,Ge}(grade)/kT}\right]\right\} \tag{8}$$

Due to the inverse relationship between the emitter charge storage delay time and $ac\beta$, τ_e is reduced for the SiGe HBT.

$$\frac{\tau_{e,SiGe}}{\tau_{e,Si}} \simeq \frac{J_{C,Si}}{J_{C,SiGe}} = \frac{1 - e^{-\Delta E_{g,Ge}(grade)/kT}}{\widetilde{\gamma}\widetilde{\eta}\frac{\Delta E_{g,Ge}(grade)}{kT} e^{\Delta E_{g,Ge}(0)/kT}} \tag{9}$$

From Equation 7, it is clear that the reductions of both τ_b and τ_e will increase the f_T of the SiGe HBT over the Si BJT. The maximum oscillation frequency is given by:

$$f_{max} = \sqrt{\frac{f_T}{8\pi C_{cb} r_b}} \tag{10}$$

where r_b is the *ac* base resistance and C_{cb} is the collector-base capacitance. The increase in f_T as well as a reduction in r_b aid in improving the f_{max} of the SiGe HBT.

1.4 Summary

This chapter introdues the fabrication aspects and the device physics that govern the operation of the SiGe HBT BiCMOS technology. The technology utilises bandgap engineering to provide significant advantages over the Si BJT including increased β, V_A, f_T, and f_{max}. Along with the high-performance SiGe HBTs, this technology provides passive component capabilities combined with deep sub-micron CMOS for system-on-a-chip (SoC) integration.

In this thesis, Chapter II provides an understanding of device mismatch and its effects on circuit performance. This chapter examines the geometric dependence of collector current variation in SiGe HBTs. Chapter III of this thesis provides a general understanding of the radiation concepts and terminology associated with radiation physics. The effect of proton radiation on SiGe HBT technology is examined along with transistor mismatch as a crucial design issue in space-borne precision analog circuits. Chapter IV explores the dependence of device mismatch with respect to temperature. Chapter V presents conclusions of the work presented in this thesis as well as suggestions for future directions for this research.

CHAPTER II

CHARACTERIZING MATCHING

2.1 Introduction

Random device mismatch plays a key role in designing precision analog circuits. In general, transistor "mismatch" refers to the measurable differences in electrical characteristics (e.g., I_C, β, or g_m) between two identically designed and layed-out devices, which are biased identically, and placed in very close proximity on the wafer to minimize cross-wafer process variations (this is often called a "matched pair"). Matched pairs are critical in many types of analog circuits, including differential pairs for the input stages of amplifiers, current mirrors for biasing, and in various circuits topologies utilizing integer multiples of identical components such as bandgap references, ADCs, DACs, and filters. Thus, accurate transistor matching is at the very heart of robust analog circuit design. In CMOS, transistor matching is a serious design constraint due to device-to-device threshold voltage variations, and in general it is well known that bipolar transistors, due to the nature of their vertical transport, have superior matching properties compared to MOSFETs, typically making bipolar-based analog circuit design in some sense simpler. To circumvent the deleterious effects of mismatch on circuit performance, designers typically use much larger than minimum-sized transistors to reduce parameter variations, but at an undesirable and signifiant performance loss.

2.2 Matching Concepts

Historically, mismatch has been treated as an ôartö rather than a science, relying on past experience and unproven or uncharacterized effects. [5] classifies the different types of variations associated with mismatch. Changes in process and device parameter variations

due to manufacturing variations are categorized as systematic or random variation. These variations can occur from lot to lot, wafer to wafer, die to die, and device to device. In certain manufacturing variations lot-to-lot and wafer-to-wafer variations are common to all devices in the circuit. An example of such a variation could occur due to over-etching. In this scenario, all transistors have a shorter than nominal length in the lot/wafer. Such variations cause a systematic shift in the device characteristics and hence, the circuit performance. However, circuit designers can overcome these issues by using differential circuit topologies and proper biasing techniques. These techniques desensitize the affect of systematic variations in an integrated circuits performance. Systematic variation can also occur due to processing gradients [6] which are independent of device size. Their impact on circuit performance can be minimized if not eliminated using layout techniques that utilize device symmetry, e.g., common-centroid structures.

In a nutshell, designers utilize 'smart' layout techniques in order to nullify the effects of systematic variation within devices. However, not all variations can be predicted during the design phase. Certain device-to-device variations, e.g., the number of dopant atoms under the gates of identical MOS transistors differs randomly, result in random differences between the device characteristics and are commonly called device mismatch. Since these variations are dependent on the device size and improve with increasing device size, circuit designers usually use larger device dimensions (area, width, length) to control the matching.

2.2.1 MOS Devices

Extensive research has been conducted in order to understand the device mismatch of two closely spaced, identical MOS transistors for different device sizes down to the deep-submicron devices [9], [10]–[15]. The experimental data in open literature shows that threshold voltage differences (ΔV_T) and current factor differences ($\Delta\beta(\beta = \mu C_o x \mathrm{W/L})$) are the dominant sources underlying the drain-source current or gate-source voltage mismatch for a matched pair of MOS transistors. These random differences have a normal distribution

with zero mean and a variance dependent on the device area WxL.

$$\sigma^2(\Delta V_T) = \frac{{A_{VT}}^2}{WL} \tag{11}$$

$$\sigma^2(\Delta V_T) = \frac{{A_{VT}}^2}{WL} \tag{12}$$

In 11, 12 the gate-width W and the gate-length L, and the proportionality constants A_VT and A_β are technology-dependent. Given the fact that V_T and β have some common process parameter dependencies, they can be modeled as independent random variables [12], [13], [17]. This is due to the fact that there is very low correlation between δV_T and $\delta\beta$ as shown by experimental data in the literature.

Most mismatch data and models presented in literature have been characterized for devices performing in strong inversion in the saturation or linear region. However, some studies for devices operating in weak inversion have also been conducted [18]-û[20]. Assuming similar experimental conditions, the device mismatch in all operating regions can be mainly attributed to V_T and β variations. Hence the source of mismatch and their matching scales with device area which is a similar trend realized in this area of study.

In studying the effects of mismatch, device layout styles, device position and orientation typically do not strongly influence the random variations between devices but can introduce strong systematic differences [21]. As a result, efficient analog layout practiced counter these effects by using dummy devices, maintaining the same current direction, the use of symmetric layouts to cancel processing gradients (e.g., common-centroid layouts for large devices), avoiding metal coverage, and maintaining identical metal fill patterns around the devices. Packaging induced stress can also introduce systematic device mismatches which can be avoided by changing the circuitÆs location on the die.

2.2.2 Bipolar Devices

In case of bipolar transistors, mismatch studies for a pair of identical, closely spaced transistors is focused mainly on variations in collector current, base current, and bias voltage (V_BE) [4], [5]. Since most analog applications require biasing the transistor in the ideal operation region (spanning several orders of magnitude in current), the study is conducted for the ideal bias region. The experimental data in open literature shows that the relative base current mismatch and the relative collector current mismatch are independent of the bias point. The matching improves with increasing emitter area and can be modeled as follows:

Unlike MOS transistors, the physical causes of bipolar mismatch have not been as extensively studied. Mismatch models based on analytical derivations or device simulation studies have not been found in the open literature [5]. In [4] the physical causes for bipolar mismatch have been studied experimentally. The dominant causes are technology dependent and include variations in the base sheet resistance, the base-emitter current densities and the emitter size. The intrinsic matching of bipolar devices is very good so that careful layout techniques such as the use of dummy devices, avoiding metal coverage, and maintaining identical environments around devices, are even more essential to avoid matching degradation and achieve this high intrinsic matching in practical circuits.

2.3 Mismatch Measurements

2.3.1 Design of Test Structures

The matching test structures were drawn symmetrically with identical metal traces to ensure that the parasitic resistances and capacitances for both the devices were equal. The devices were oriented to allow current flow in same direction, and the center-to-center distance between the devices was kept constant for all the geometries used. The structure had common emitter and base pads to ensure identical bias conditions and eliminate differences caused due to contact resistance between the probe and bond pad. The collector pad

Table 2: Matched-Pair Device Geometries Investigated.

Device Size(μm^2)	Devices in Parallel
$0.4 \times 1.4\mu$m^2	1
$0.4 \times 5.0\mu$m^2	1
$0.4 \times 10.0\mu$m^2	1
$0.4 \times 10.0\mu$m^2	2
$0.4 \times 10.0\mu$m^2	4
$0.4 \times 10.0\mu$m^2	8

contacts were laid out individually to avoid fluctuations due to junction leakage current [4]–[5]. Precautions were taken to avoid metalization over the transistors under test [22]. Figure 7 a) shows a schematic representation of the matching structures, and Figure 7 b) shows the layouts of several of the different device geometries (Table 2) utilized in the investigation. We focus here on collector current (I_C) mismatch under fixed V_{BE} conditions.

2.3.2 Results

Mismatch fluctuations are characterized based on statistical distribution of differences between measured electrical variables. The work focuses on collector current offsets ($\Delta I_C/I_C$) as a function V_{BE}.

$$\Delta I_C/I_C = \frac{(I_{C1} - I_{C2})}{I_{C1}} \tag{13}$$

Figure 10 shows values of $\Delta I_C/I_C$ for four different devices plotted with respect to V_{BE}. The plot illustrates the fact that at low V_{BE} bias (0.6 to 0.75V), $\Delta I_C/I_C$ remains nearly constant. In this low current range, the SiGe HBT operates ideally (ideal part of the forward-active Gummel characteristics (Figure 8)). As the bias voltage increases, $\Delta I_C/I_C$ deviates from its constant behavior, due to high current effects and series resistance fluctuations. As a result, the $\Delta I_C/I_C$ values are extracted from the ideal region; a region where mismatch-sensitive precision analog circuit would likely be biased. Figure 11 shows the statistical distribution for the $0.4\times10.0\mu$m^2 device. The histogram follows Gaussian-like distributions, suggesting that although the sample size is limited (15 devices), it displays the expected

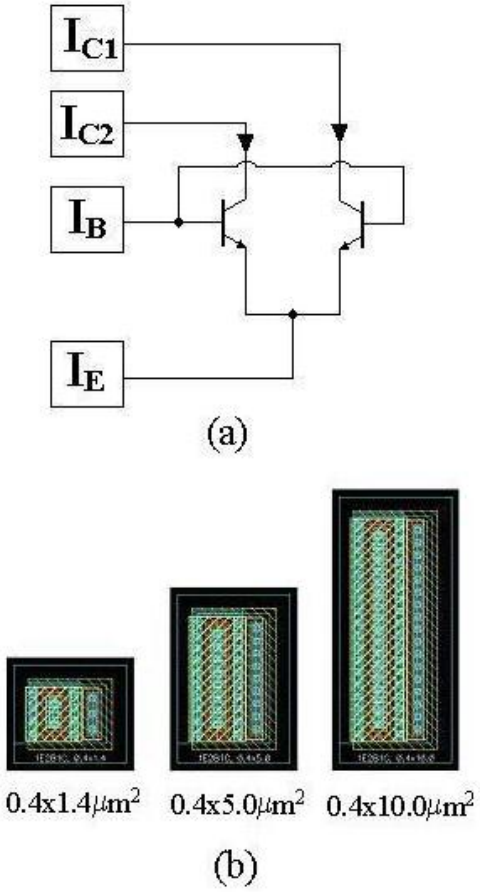

Figure 7: (a) Circuit representation of the matching structures;(b) Device geometry available.

statistical behavior of classical mismatch, as shown in [7].

In order to quantitatively assess the mismatch fluctuations in these SiGe HBTs, the standard deviation of the collector current offsets are scaled with respect to emitter area. Under the conditions given in [7] the standard deviation of the offset is theoretically inversely proportional to the square root of the active area of the matched component, according to:

$$\sigma_{\Delta P/P} = \frac{A_{\Delta P/P}}{\sqrt{WL}} \tag{14}$$

$A_{\Delta P/P}$, the so-called "A-factor," is the mismatch fluctuation performance factor used to facilitate mismatch comparisons between device geometries as well as different technologies. Referring to Figure 12, the A-factor for the devices is about 4%μm.

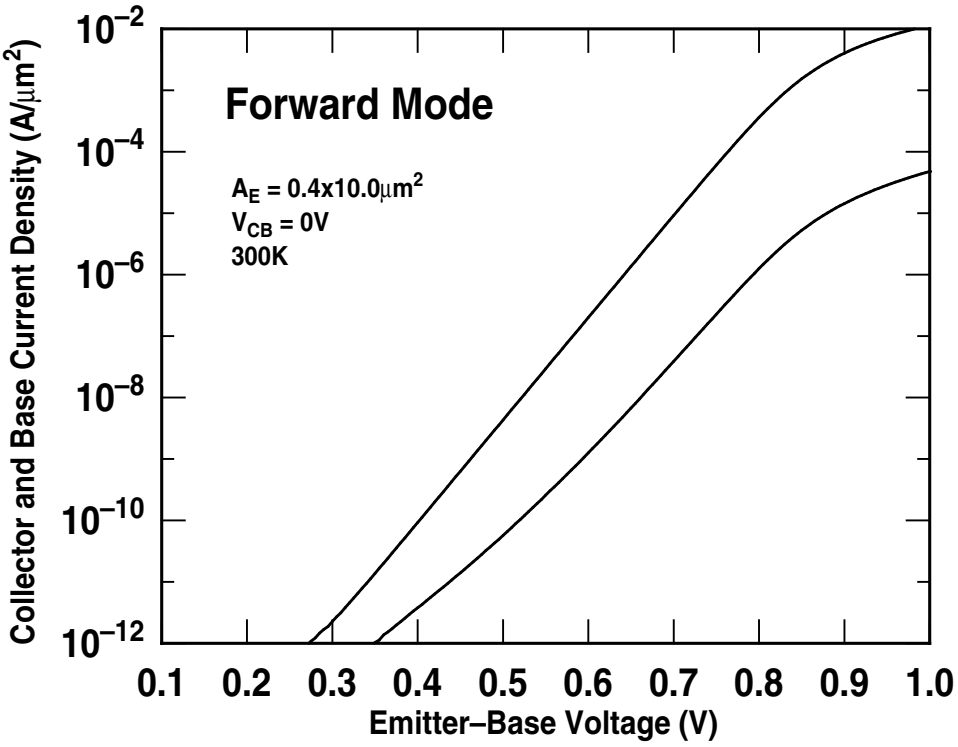

Figure 8: Forward-mode Gummel characteristics.

The observed linear behavior can be attributed to the fact that as device size increases, the random component of the mismatch decreases. However, the 0.4x1.4μm^2 device proves to be an anomaly to the trend. In this case, current fluctuations can be attributed to gradient offsets [6]. These offsets become more prevalent as the minimum separation distance increases. In the case of smaller devices, the minimum separation distance will be higher in order to maintain the same center-to-center spacing between the test devices.

2.3.3 Summary

In order to comprehend the detrimental effects of mismatch on circuit design, it is essential to understand the underlying effects that influence device mismatch and isolate the root causes. This section provided an insight into current mismatch as a function of geometry in SiGe HBTs. The A-factor can be used to describe mismatch fluctuations for the given technology to variations in emitter size. This can be particularly useful in analog circuit

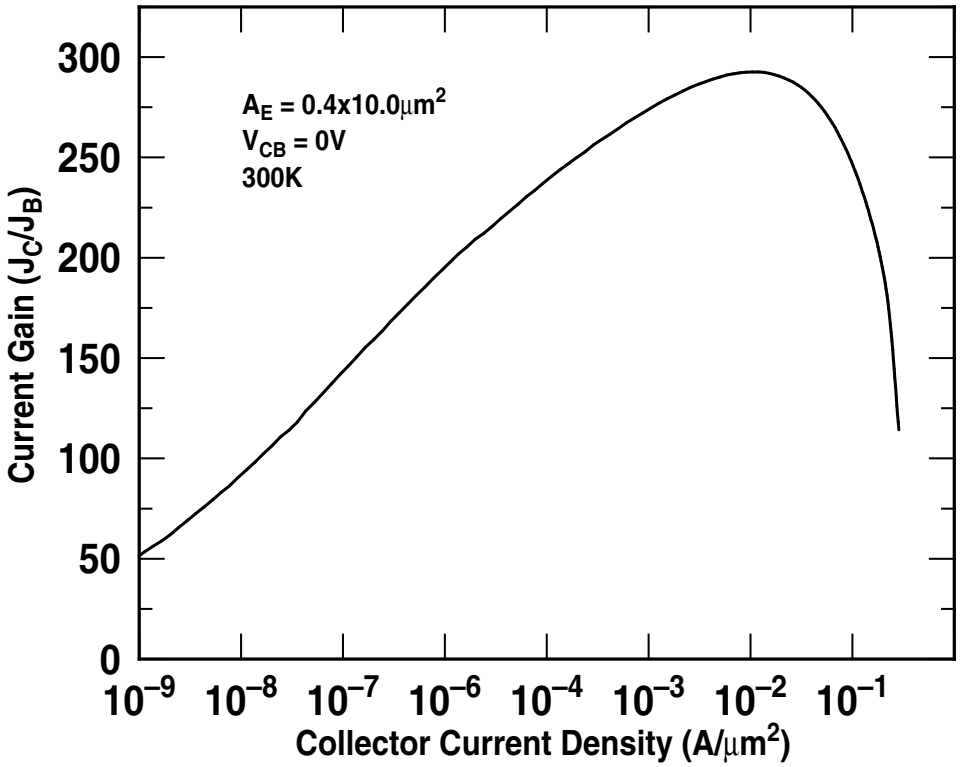

Figure 9: Current gain.

blocks that are dependent on the availability of matched pairs. In later sections, the effects of proton exposure and high temperature on mismatch fluctuations in SiGe HBTs is studied.

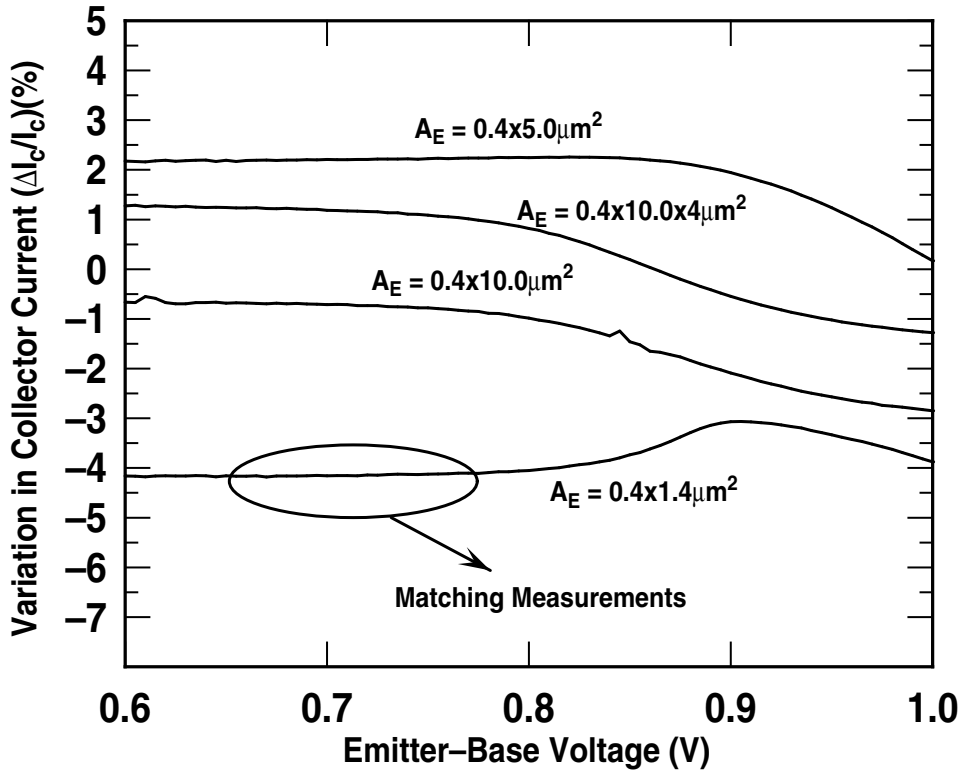

Figure 10: Collector current variation as a function of emitter-base bias for a variety of device geometries.

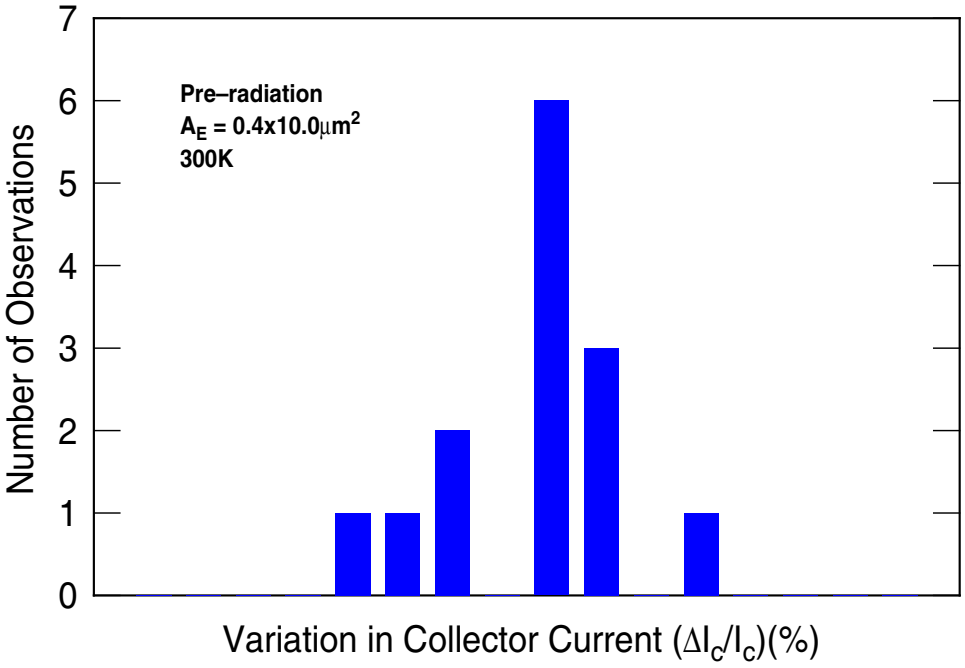

Figure 11: Collector current variation histogram.

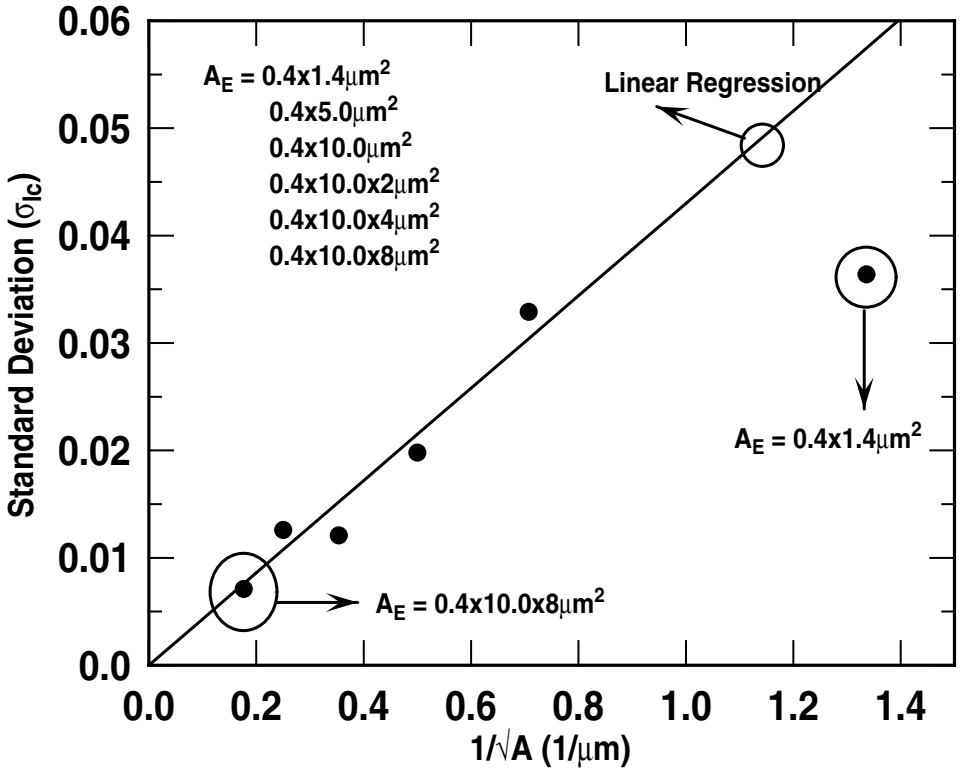

Figure 12: Standard deviation of the collector current variation as a function of the reciprocal of the square root of the area.

CHAPTER III

RADIATION EFFECTS

3.1 Introduction

Today, the challenges associated with electronic systems in space missions forms a major research area. The study of radiation tolerance is very important since electronic systems need to operate efficiently under the harsh radiation conditions of the space environment. Factors such as orbital path, altitude, and duration of flight are involved in determining the conditions encountered in the mission. Since these conditions vary with every mission, modeling devices and circuits to perform well in these conditions is a difficult, yet crucial task. This suggests that device, circuit, and system designers must have a basic understanding of the radiation environment and its effects on devices and circuits. This chapter provides an overview of the space radiation environment, basic terminology, and an understanding of the radiation damage mechanisms.

3.2 Radiation Concepts and Damage Mechanisms

The metric used to quantify the amount of energy an energetic particle or photon deposits in a particular material is *rad* ("radiation absorbed dose") where

$$1 \text{ rad} = 100 \text{ ergs/gram} = 6.24 \times 10^{13} \text{ eV/gram} \tag{15}$$

The SI unit for total ionizing dose is the grey (Gy) where

$$100 \text{ rad} = 1 \text{ Grey(Gy)} = 1 \text{ J/kg} \tag{16}$$

Since the energy absorbed depends on the density of the material, the rad is a material dependent property. Thus, when using the rad unit, the target material must also be specified.

For Si based electronics, typical units are rad(Si) or rad(SiO_2), where 1.000 rad(SiO_2) = 0.945 rad(Si).

As stated earlier, the space environment contains a mixture of particles detrimental to devices and circuits. The Earth's magnetosphere is bombarded by a nearly isotropic flux of energetic charged particles, primarily the nuclei of atoms stripped of all electrons. These comprise 85% protons (hydrogen nuclei), 14% a -particles or helium nuclei, and 1% heavier ions covering the full range of elements. Regions of radiation trapped in the Earth's magnetic field form belts known as Van Allen belts. Research in this field showed that these divide into two belts. The inner belt extends to 2.5 Earth radii and the outer belt extends to about 10 Earth radii. The former comprises of energetic protons up to 600MeV together with electrons up to several MeV, and the latter comprises of mainly of electrons and a small quantity of soft protons (0.1 to 5 MeV). The slot region between the belts has lower intensities but may be greatly enhanced for up to a year following one or two solar events in each solar cycle. The outer belt is naturally highly time-variable and is driven by solar wind conditions. An illustration of the interaction between the solar wind and the Earth's magnetic is shown in Figure 13.

During solar maximum, the sun contributes to radiation in the space environment. Events such as solar flares and/or subsequent coronal mass ejections (CME) accelerate lower energy particles. These solar particle events comprise both protons and heavier ions and last for several days and tend to vary in composition from event to event. Energies typically range up to several hundred MeV and have most influence on high inclination or high altitude systems.

Galactic cosmis rays also contribute to radiation in the space environment. The primary cosmic rays interact with air nuclei to generate a cascade of secondary particles comprising protons, neutrons, mesons and nuclear fragments. The intensity of radiation builds up to a maximum at 18km (Pfotzer maximum) and then slowly drops off to sea level. At normal aircraft cruising altitudes the radiation is several hundred times the ground level intensity

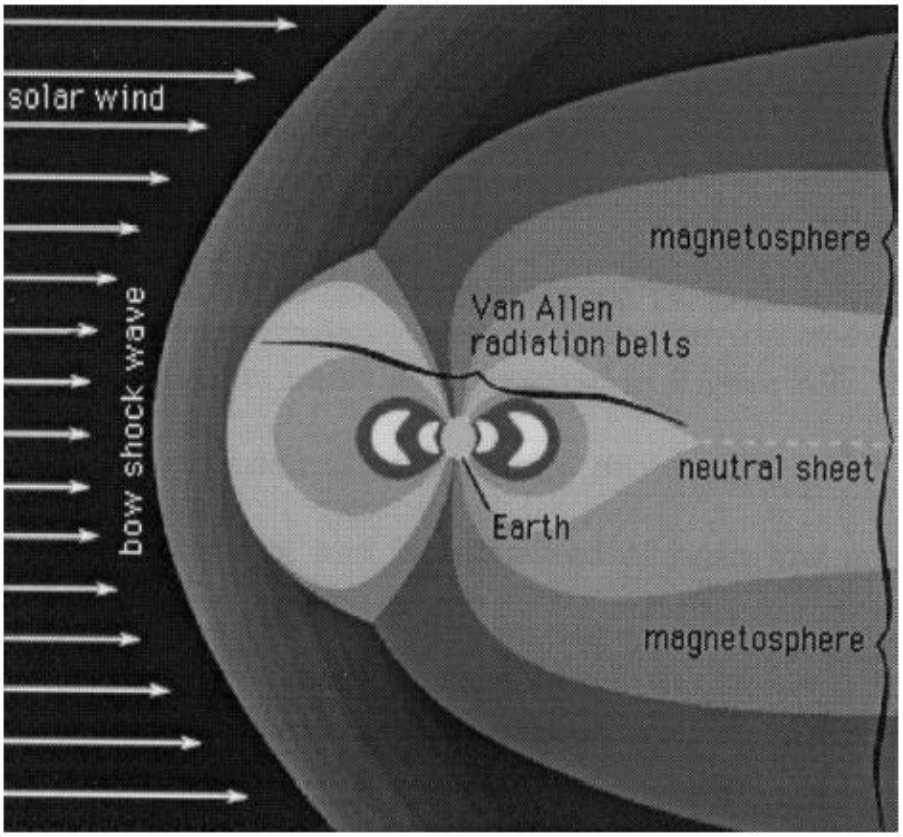

Figure 13: Illustration of the solar wind and radiation belts surrounding the Earth.

and at 18km a factor three higher again. Solar particles are less penetrating and only a few events in each cycle can reach aircraft altitudes or ground level. Some of the neutrons are emitted by the atmosphere to give a significant albedo neutron flux at low earth orbital (LEO) spacecraft. It is the decay of these albedo neutrons into protons that is believed to be the source of the inner radiation belt.

Given the harsh space conditions, electronic systems malfunction due to two major damage mechanisms : ionization damage and displacement damage. TID ionization and displacement damage are examined in this section [1], [26], [27], [28].

Total ionizing dose creates electron-hole pairs within dielectric layers (oxides, nitrides etc.) and subsequent generation of traps at or near the interface with the semiconductor or of trapped charge in the dielectric. This can produce a variety of device effects such as flatband and threshold voltage shifts and surface leakage currents. Ionization effects depend on a number of parameters including the linear energy transfer (LET) of the particle. The LET is defined as the energy transferred per unit of path traveled by the ionizing particle normalized by the density of the target material. Both the particle's LET and the applied electric field influence the rate of recombination of electron-hole pairs. The dose-rate influences the relative importance of hole traps and interface states. Since ionization damage occurs primarily in isolating oxides and in oxide-semiconductor interfaces, the dose should be defined in relationship to the material affected to avoid errors caused by considering average doses. Another factor to consider is radiation-induced conductivity, which is important in mitigating charging of dielectric materials. There are several factors that need to be considered for total dose effects. TID depends on device bias during irradiation and annealing effects.

Displacement damage mechanisms also needs to be considered in unhardened devices to devise a model for space based electronic systems. Energetic particles such as neutrons, protons, electrons, alpha-particles and heavy ions can create damage in devices by displacing atoms in the crystal lattice. High-energy protons also lead to production of secondary

electrons which can cause displacement effects. The displacement creates stable defect states within the bandgap giving rise to certain effects depending on the temperature, carrier concentration and the location at which the defect resides. The presence of defects can lead to generation of electron-hole pairs, increasing the leakage current in devices. Defects can also cause ecombination of electron-hole pairs, affecting carrier lifetimes and hence the dynamic response. Another effect involves trapping of carriers, leading to loss in charge transfer efficiency in charge-coupled devices in case of minority carrier trapping or carrier removal in case of majority carrier trapping. Defecs can also lead to compensation of donors or acceptors by defect centers. Defects can cause increased current in reverse biased junctions - particularly for small bandgap materials and high electric fields by tunelling of carriers.

Radiation damage affects the performance of various semiconductor devices in different ways. This is due to differences in device operation and fabrication. This section reviews the effects of radiation damage on both Si bipolar transistors and CMOS devices [1], [26], [27]. However, the inherent robustness to ionizing radiation makes SiGe technology attractive for many space system applications. Recent studies have reported the proton tolerance of SiGe HBTs for a variety of different SiGe BiCMOS technologies [1], [31]. This work investigates the proton radiation response of the National BiCMOS8 SiGe HBT process technology it also investigates, for the first time, the radiation-induced changes in parametric mismatch fluctuations of SiGe HBTs in identically designed SiGe HBT matched pairs with different emitter geometries.

3.3 Radiation Effects in SiGe HBTs

The devices used for the study were the standard devices as shown in Table 2. The test structures were irradiated with 63.3 MeV protons at the Crocker Nuclear Laboratory at the University of California at Davis. The dosimetry measurements used a five-foil secondary emission monitor calibrated against a Faraday cup. The radiation source (Ta scattering

foils) located several meters upstream of the target establish a beam spatial uniformity of about 15% over a 2.0 cm radius circular area. Beam currents from about 20 nA to 100 nA allowed testing with proton fluxes from 1×10^9 to 1×10^{12} proton/cm^{2}sec. The dosimetry system has been previously described [29], [30], and is accurate to about 10%. At a proton fluence 5×10^{13} p/cm^2, the measured equivalent total ionizing dose was approximately 6,759 krad(Si). The SiGe HBTs were irradiated with all terminals floating, which is known to present worst case conditions for radiation damage [32]. The structures were measured at room temperature with an Agilent 4155 Semiconductor Parameter Analyzer. The radiation exposure and testing conditions were the same for all of the devices measured to facilitate ambiguous comparisons.

3.3.1 *dc* Results

The forward-mode Gummel characteristics for a SiGe HBT subjected to a 63 MeV proton fluence of $5x10^{13}$ p/cm^2 is shown in Figure 14. Exposure to high proton fluences produces G/R trapping centers at the emitter-base spacer oxide around the periphery of the transistor [33]. The increase in base leakage current causes a significant degradation in current gain (β), as seen in Figure 15.

As a result of irradiation, a slight increase in the collector current is observed between the matched pairs, as shown in Figure 14. The proton displacement damage in the volume of the transistor induces a decrease in the net base charge density, which in-turn causes the neutral base boundary on both the emitter and collector sides of the base to shrink. This reduces the base Gummel number, increasing the collector current. The National BiCMOS8 SiGe technology is reasonably tolerant to proton radiation (up to Mrad-level equivalent dose), without any intentional radiation hardening, as indicated by the above results.

Similar to the devices measured pre-radiation, the irradiated samples statisticaly follow a Gaussian-like distribution as shown in Figure 17. Hence, it suggests that although the

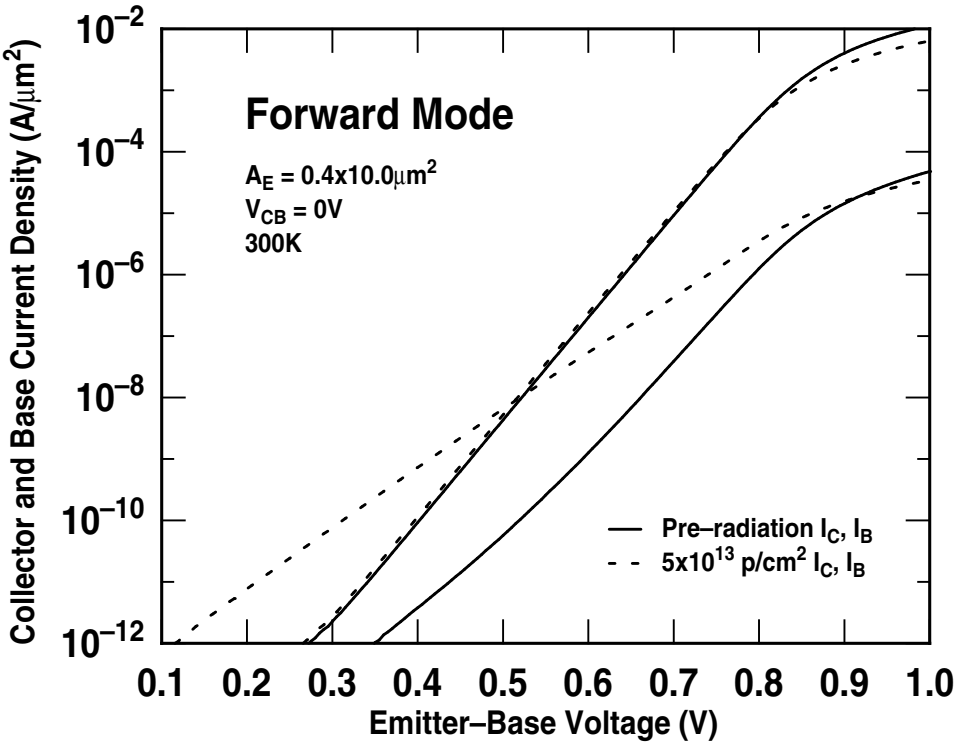

Figure 14: Forward-mode Gummel characteristics before and after irradiation.

sample size is limited (15 devices), it displays the expected statistical behavior of classical mismatch, as shown in [7]. Referring to Figure 18, there is negligible difference between the A-factor for the pre-radiated and post-radiated devices, 4%μm and 4.1%μm respectively.

Comparing the pre-radiated and post-radiated data, there is little observed change in the standard deviations. Although the collector current slightly increases, the $\Delta I_C/I_C$ remains approximately the same. This trend can be observed in the magnified version of the Gummel characteristics shown in Figure 19. To probe this more deeply, Figure 20 shows the correlation between the pre-radiated and post-radiated data. From the graph it is evident that radiation has little or no effect on collector current mismatch fluctuations, since the linear regression through the points results in a unity slope (i.e., well correlated). This lack of radiation-induced change is clearly good news from an analog circuit design perspective.

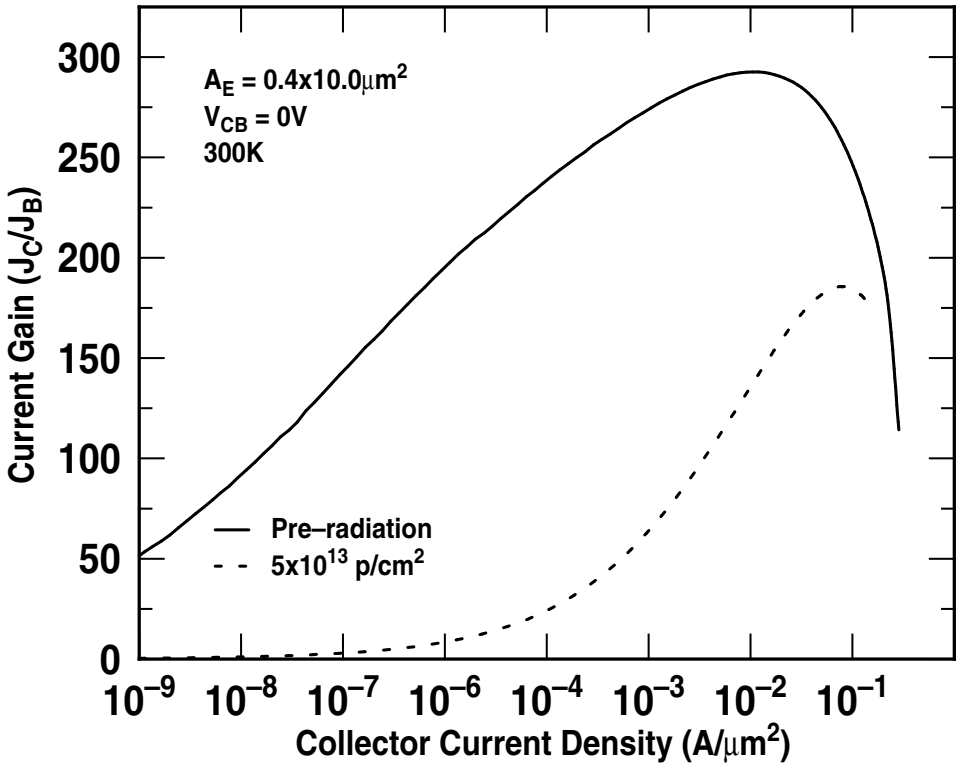

Figure 15: Current gain degradation before and after irradiation.

3.3.2 Summary

This chapter provides an insight into the types of radiation encountered in the space environment and its effects on device and circuit performance via various damage mechanisms. Furthermore, it provides an understanding of the effects of proton irradiaion in SiGe HBTs and for the first time, the effects of proton exposure on mismatch fluctuations in SiGe HBTs. The change in collector current (I_c) variation is negligible after $5x10^{13}$ p/cm^2 proton fluence, indicating that collector current mismatch should not be a major issue for space-borne analog circuits utilizing SiGe HBTs.

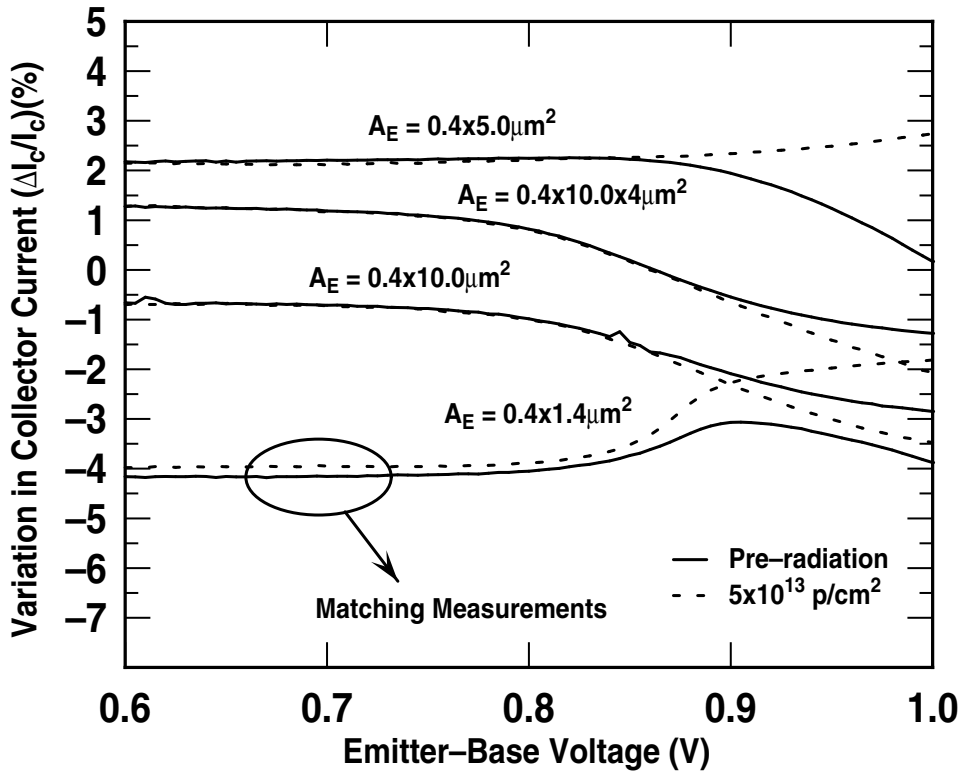

Figure 16: Collector current variation as a function of emitter-base bias for a variety of device geometries.

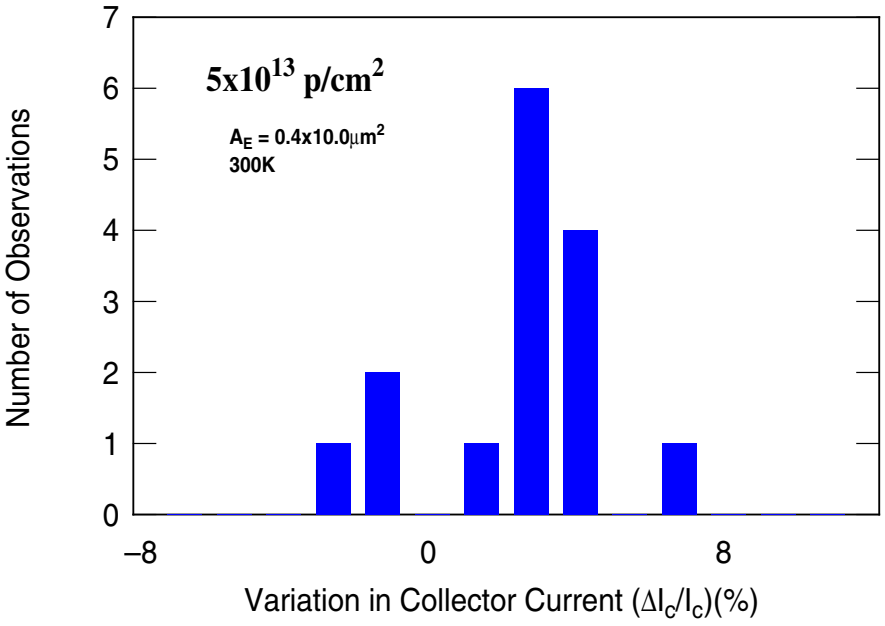

Figure 17: Collector current variation histogram - post-radiation.

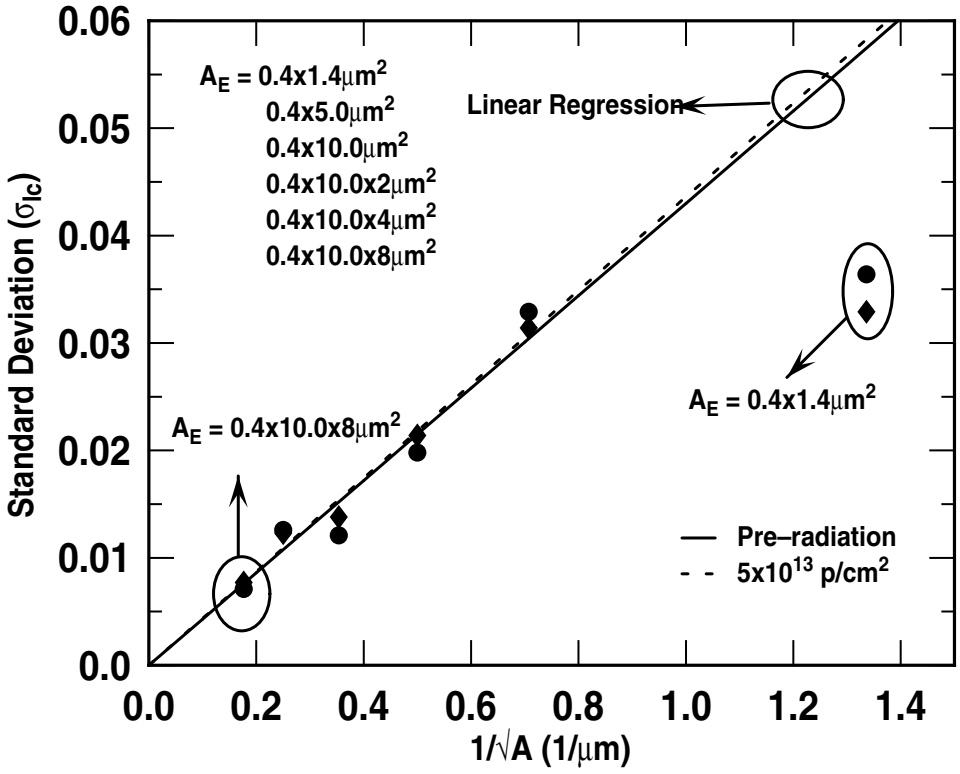

Figure 18: Standard deviation of the collector current variation as a function of the reciprocal of the square root of the area.

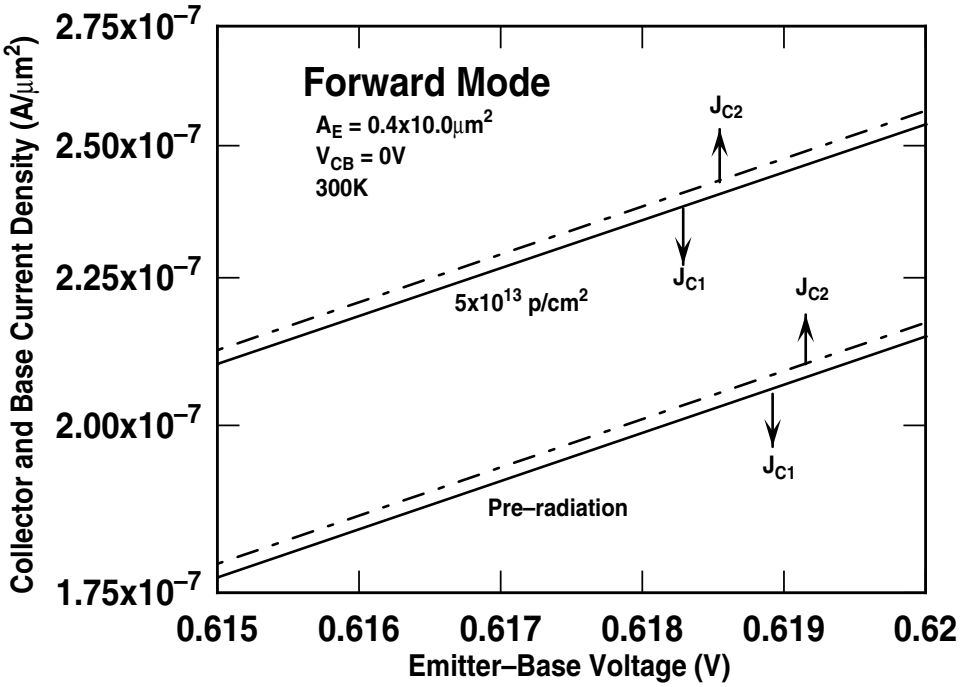

Figure 19: Collector currents for each transistor of the matched pair for both pre-radiation and post-radiation.

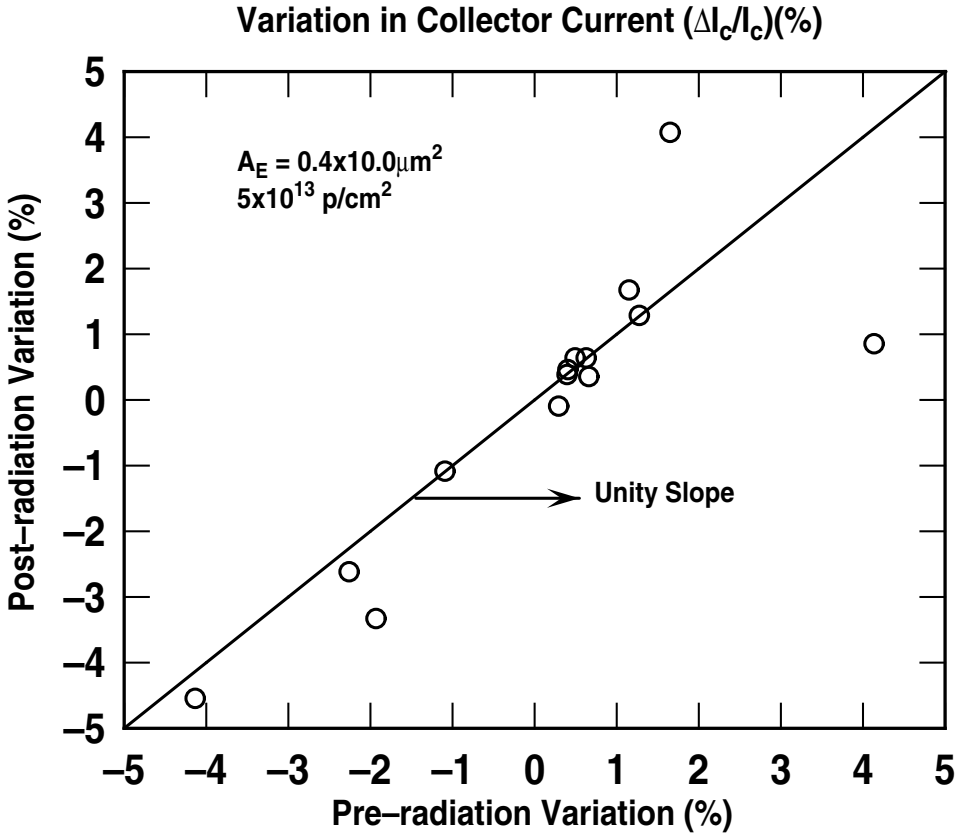

Figure 20: Correlation of collector current variation between pre-radiation and post-radiation.

CHAPTER IV

TEMPERATURE MISMATCH EFFECTS

4.1 Introduction

Given the expanding realm of electronic systems applications, research conducted in high-temperature electronics has gained popularity with applications such as automobiles, heavy vehicles, power switching, engine electronics, aerospace (e.g., the ôall electric aircraftö), shipping, oil well logging, nuclear power, planetary space missions, and radar systems [41]. Several technologies have been used in these applications including SOI CMOS, GaAs, and SiC. Traditional Si CMOS and bipolar transistor operations are typically limited to temperatures below 200 C due to junction leakage currents [45] and reliability concerns. These issues occur since these transistors use reverse-biased p-n junctions for electrical isolation. However, these device technologies require extensive (costly) modification in order to provide consistent performance at high-temperatures.

SiGe HBT BiCMOS technology has recently attracted interest because of its inherent advantages over Si bipolar transistors and its growing applications in analog, RF, digital, and microwave applications. As stated earlier, SiGe HBTs utilizes efficient bandgap engineering that favors cryogenic operations while causing degradation in device performance at higher temperatures. However, [39] and [40] demonstrates that, contrary to popular opinion, SiGe HBTs are potentially well-suited for many high temperature electronics applications.

4.2 High Temperature Concepts

There are several challenges associated with high-temperature electronic applications with transistor reliability being most crucial [42], [43]. A major concern in p-n junction devices is the increase in junction leakage current with increasing temperature. This effect can be

attributed to the thermal generation of carriers in the junctions.

Thermal generation of carriers depends exponentially on temperature and bandgap (kT/E_g). As shown in Figure 21a, thermal excitation provides electrons with enough energy to move from the valence band to the conduction band (direct thermal generation). However, thermally assisted generation of carriers with R-G centers acting as intermediaries can be seen in Figure 21b. As a result, as temperature increases, the leakage current increases. In case of devices with larger bandgaps, the probability of an electron moving from the top of the valence band into the conduction band is lower. As a result, the electrons require higher energy to jump across the gap, lowering the leakage current. However, since the bandgap is also dependent on temperature, the band gap energy decreases as the temperature increases. Thus, at elevated temperature, leakage current increases. Another factor that affects thermal generation depends on whether the semiconductor has a direct or indirect bandgap. Consequently, generation of carriers in the junctions will be more rapid for direct than for indirect bandgap semiconductors for a given bandgap. Zipperian [42] sets a maximum acceptable leakage current (0.1 A/cm^2), and hence provides a range of operation for the various technologies at high-temperature.

Another physical effect that impacts high-temperature performance in p-n junction transistors is an increase in the intrinsic carrier density with temperature. For an intrinsic semiconductor, we can write,

$$n_i = 2\pi kT/h^{2^{3/2}} m_h {m_e}^{3/4} e^{-E_g/2kT} \tag{17}$$

where E_{g0} is the energy gap, E_C û E_V, k is the Boltzmann's constant, h is the Planck's constant, and m_e and m_h are the electron and hole effective masses respectively. The strong dependence of the carrier concentration on bandgap and temperature is evident from Equation **??**. The smaller the bandgap, the greater the probability of an electron moving from the top of the valence band into the conduction band, since less energy is required for the electron. Similarly, the higher the temperature of a device, the greater

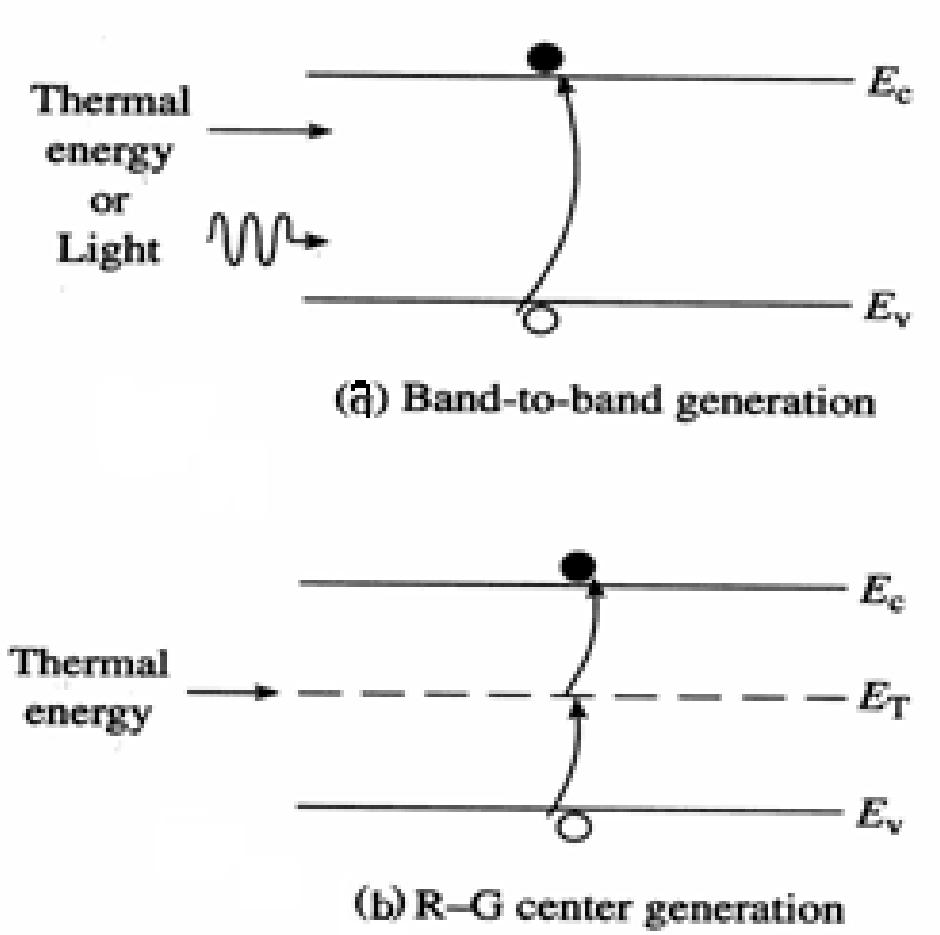

Figure 21: Energy band visualization of thermal generation processes.

the energy imparted to the electrons in the valence band, and hence larger the number of electrons that have the sufficient energy to jump across the gap. Thus electron and hole densities increase with temperature and decrease with increasing E_g. As the temperature increases, the increased thermal energy ionizes significant numbers of the semiconductor atoms themselves (for example the Si atoms) in addition to the dopant atoms. This contributes additional electrons and holes in the conduction and valence and bands and, more important, results in approximately equal numbers of carriers in each band, independent of the doping, resulting in a condition called intrinsic. Since there are orders of magnitude more semiconductor atoms than dopant atoms, the influence of the dopant is overwhelmed at a sufficiently high temperature and hence, the junctions are ôwashed outö.

In most situations, circuits designed to operate at high-temperature are also required to perform efficiently over a wide range of temperatures. Several device parameters such as Fermi level, intrinsic carrier density, carrier generation rate, and carrier mobility depend on temperature [46]. This causes certain device characteristics to vary with temperature, causing variance in conductances, transconductances, leakage currents, diode voltage drops, and FET threshold voltages. Reliability also forms a central issue for high-temperature circuit operation because high temperature accelerates many device and circuit wearout mechanisms. As a result, in order to attain required circuit performance over a wide temperature range, designers need to understand the physical and electrical behavior for the entire temperature range.

Device mismatch has been a deterrent to obtaining optimum circuit performance in precision analog circuits at room temperature. Certain applications such as oil drilling require ADC to operate efficiently at high temperatures. As such, device mismatch effects at high-temperature have not been seriously studied. This is probably because the temperature effects are believed to be insignificant to transistor mismatch. Hence, none of the mismatch models existing today include temperature effects. However, results presented in [44] for MOS mismatch, suggest a noticeable improvement in drain current and threshold voltage

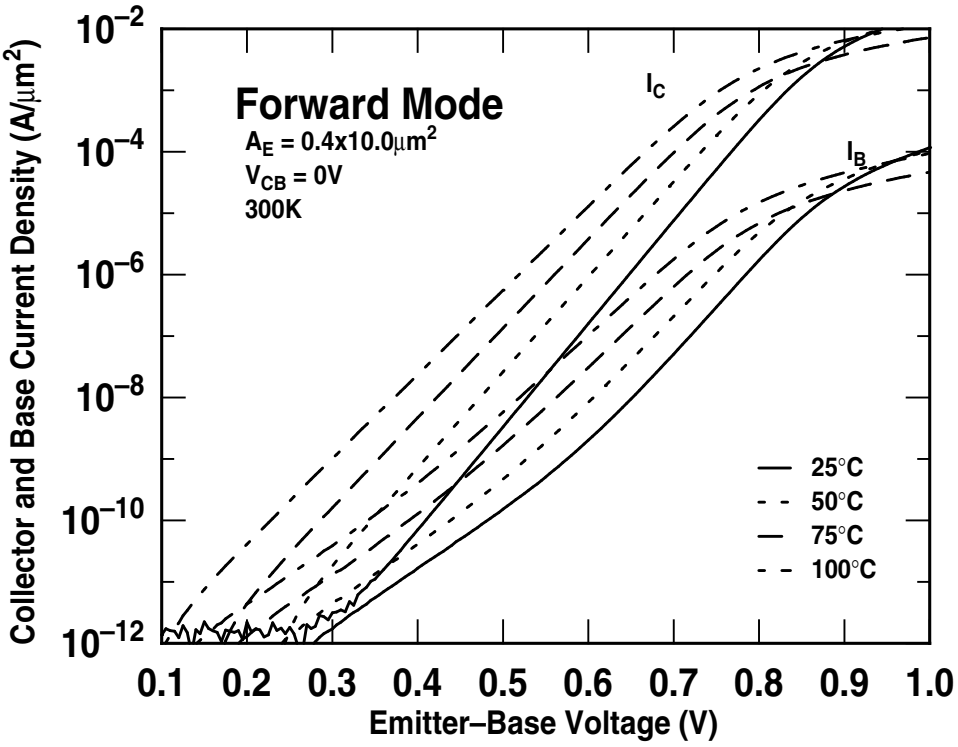

Figure 22: Forward-mode Gummel characteristics as a function of temperature.

mismatch as temperature increases. This work investigates the effect of high-temperature on transistor mismatch in SiGe HBTs, for the first time, in order to demonstrate their applicability in high-temperature precision analog circuits.

4.3 Temperature Effects

4.3.1 Results

The devices used for the study were the standard devices as shown in Table 2. SiGe HBTs were measured on-wafer using Agilent 4155 C on probe stations capable of operating 20 C to 100 C.

Figure 22 shows the the Gummel characteristics of the SiGe HBTs at 25 C, 50 C, 75 C, and 100 C. The decrease in turn-on voltage is evident from Figure 22 with increasing temperature. This effect is due to the change in the intrinsic carrier concentrations, hence, causing a decrease in the emitterûbase built-in potential.

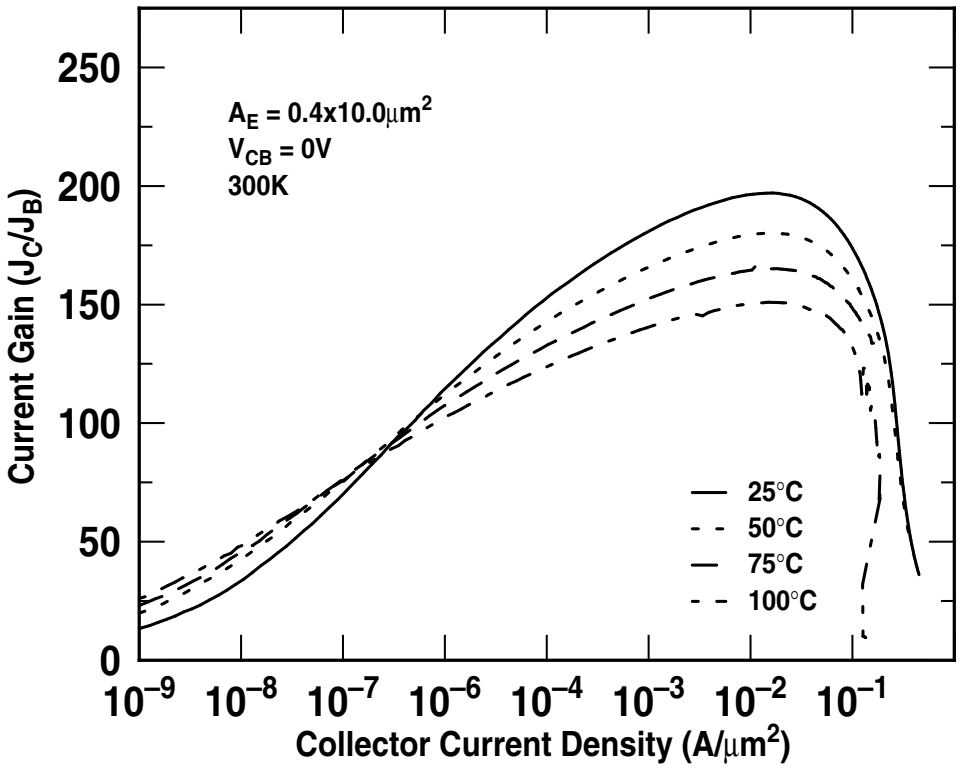

Figure 23: Current gain as a function of collector current at 25C, 50 C, 75 C, and 100C.

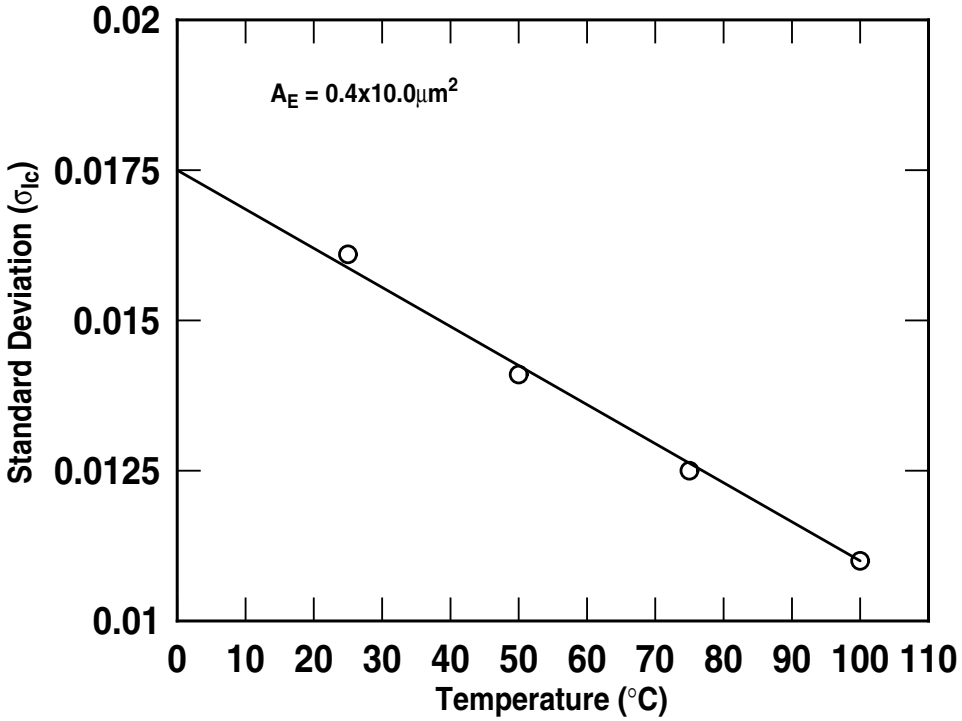

Figure 24: Standard deviation of the collector current variation as a function of temperature.

The current gain of the measured SiGe HBTs at 25 C, 50 C, 75 C, and 100 C are shown in Figure 23. As expected, the peak current gain decreases as temperature increases. Equation 4 shows the influence of temperature on β of the device. The device maintains ideality upto 100 C with current gain greater than 100. Its hould also be noted that the device has higher current drive capability at temperatures higher than room temperature. This suggests that the impact of high temperatures on the carrier mobility and hence series resistances is not detrimental to circuit performance. However, parasitic leakage caused by minority carrier generation in the collector-substrate junction could limit high temperature applications [40].

Figure 24 illustrates how the variation in collector current changes with repect to temperature. As temperature increases, the standrad deviation of the current variation decreases. Hence, at higher temperatures, collector current mismatch improves. This suggests that devices and circuits will operate closer to simulated values from the matching standpoint at the

higher temperatures. This allows designers room for experimentation in design space since it relaxes the trade-offs circuit designers need to make in order to obtain optimum circuit performance in precision analog circuits.

4.3.2 Summary

This chapter accessed the applicability of using SiGe HBTs for high-temperature analog design applications. It was observed that the Sige HBTs not only exhibit sufficient gain but also see reduced collector current variation at high temperatures. These features would promote the use of SiGe HBTs for high temperature applications.

CHAPTER V

CONCLUSION

5.1 Conclusion

The purpose of this work was to investigate the effects of device mismatch in SiGe HBT BiCMOS technology under extreme conditions such as radiation and high temperatures.

Matched pairs are critical in many types of analog circuits, including differential pairs for the input stages of amplifiers, current mirrors for biasing, and in various circuits topologies utilizing integer multiples of identical components such as bandgap references, ADCs, DACs, and filters. Thus, accurate transistor matching is at the very heart of robust analog circuit design. Chapter II explores the fundamentals of device mismatch and explores for the first time the collector current variations in SiGe HBTs. Our study indicates geometric dependence on collector current variation, as expected, the excpetion being the smallest device geometry. The computed A-factor is comparable if not better than other device technologies.

Chapter III examined the effects of radiation on various SiGe HBT BiCMOS technologies. The space community is increasingly using COTS parts in spaceborne systems, thus radiation testing on new commercial technologies is imperative. The effects of proton irradiation on matched device pairs on a new commercially-available SiGe technology were examined for the first time. We report that proton induces some damage in the SiGe HBT operating in forward-mode. However, our findings indicate that the *dc* circuit performance is total dose tolerant up to Mrad-level equivalent total dose.

Chapter IV presents the results of the effects of collector current mismatch at high temperatures. As such, device mismatch effects at high-temperature have not been seriously studied. This is probably because the temperature effects are believed to be insignificant to

transistor mismatch. However, our results suggest a noticeable improvement in collector current mismatch as temperature increases. This characteristic is essential in order to prove its applicability in high-temperature precision analog circuits.

5.2 Future Directions

The focus of this work was in obtaining in-depth understanding of collector current mismatch under different conditions. Further investigation could involve examining base current and emitter-base voltage variations under similar conditions in order to prvide a complete picture of device mismatch in SiGe HBTs. Furthermore, these measurements could be applied to a generation of technologies in order to understand the change in device mismatch with technology scaling. The results obtained in this study could also be used to generate models that account for device mismatch in order to facilitate circuit designers by providing worst condition simulations capabilities. This will allow circuit designers to account for variability in their designs.

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